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## What is claimed is:

b	A seminary desired and bigger assumption as
1 5 <sup>c</sup>	1. A semiconductor device, comprising:
2	a plurality of metal line patterns having a predetermined surface area
3	size, wherein two adjacent metal line patterns are spaced apart from each
4	other at a predetermined distance.
1	2. A semiconductor device as claimed in claim 1, wherein the
2	predetermined distance is greater than 1.0 μm.
l	3. A semiconductor device as claimed in claim 1, wherein the
2	predetermined distance is greater than 1.5 μm.
1	4. A semiconductor device as claimed in claim 1, wherein the
2	plurality of metal line patterns have a surface area size of greater than
3	"30μm×30μm".
1	5. A semiconductor device, comprising:
2	a metal line layer having a plurality of metal line patterns spaced apart
3	from each other; and
4	at least one underlying layer under the metal line layer,

wherein the space between two adjacent metal line patterns has a

sufficient width to prevent a crack from occurring in the underlying layer.

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1500	6. A semiconductor device as claimed in claim 5, wherein the
2	width of the space is greater than 1.0 μm.
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1	7. A semiconductor device as claimed in claim 5, wherein the
2	width of the space is greater than 1.5 μm.
1	8. A semiconductor device as claimed in claim 5, wherein the
2	underlying layer is an insulating layer.
1	9. A semiconductor device as claimed in claim 5, wherein the
2	metal line pattern has a surface area size of greater than "30μm×30μm".
1	10. A semiconductor device, comprising:

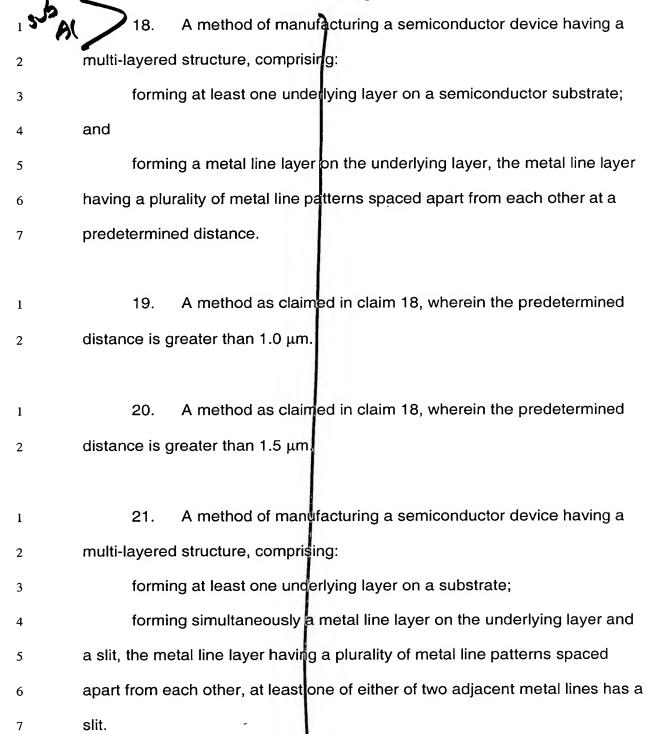
a plurality of metal line patterns, wherein two adjacent metal line patterns are spaced apart from each other and at least one of the two adajacent metal line patterns has a slit.

- 11. A semiconductor device as claimed in claim 10, wherein the slit has a width of greater than 1.0  $\mu m$ .
- 12. A semiconductor device as claimed in claim 11, wherein the slit is formed at a predetermined distance from an edge of the metal line pattern.

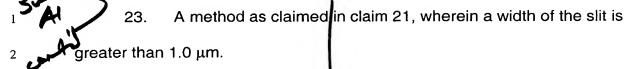
slit is less than 4.0  $\mu m$ .

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1	13. A semiconductor device as claimed in claim 12, wherein the
2	predetermined distance is less than 4 μm.
	<b>C.S.</b>
1	14. A semiconductor device having a multi-layered structure,
2	comprising:
3	a metal line layer having a plurality of metal line patterns spaced apart
4	from each other;
5	at least one underlying layer under the metal line layer; and
6	a slit formed at a sufficient distance from a space between two
7	adjacent metal line patterns to prevent a crack from occurring in the
8	underlying layer.
1	15. A semiconductor device as claimed in claim 14, wherein the slit
2	is formed in a direction parallel to the space between two adjacent metal line
3	patterns.
1	16. A semiconductor device as claimed in claim 14, wherein the slit
2	has a width greater than 1.0 μm.
1	17. A semiconductor device as claimed in claim 14, wherein the
2	distance from the space between the two adjacent metal line patterns to the

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22. A method as claimed in claim 21, wherein the slit is formed in a direction parallel to the space between two adjacent metal line patterns.



- 24. A method as claimed in claim 21, wherein a distance from the space between two adjacent metal line patterns to the slit is less than 4.0 μm.
- 25. A method of manufacturing a semiconductor device, comprising:

forming at least one underlying layer on a substrate;

forming simultaneously a metal line layer on the underlying layer and a slit, the metal line layer having a plurality of metal line patterns spaced apart from each other, the slit formed at a sufficient distance from a space between the two adjacent metal line patterns in order to prevent a crack from occurring in the underlying layer.

- 26. A method as claimed in claim 25, wherein the slit is formed in a direction parallel to the space between two adjacent metal line patterns.
- 27. A method as claimed in claim 25, wherein the width of the slit is greater than 1.0 μm.

28. A method as claimed in claim 25, wherein the distance between the slit and the space between two adjacent metal line patterns is less than 4.0 μm.